

Figure 1

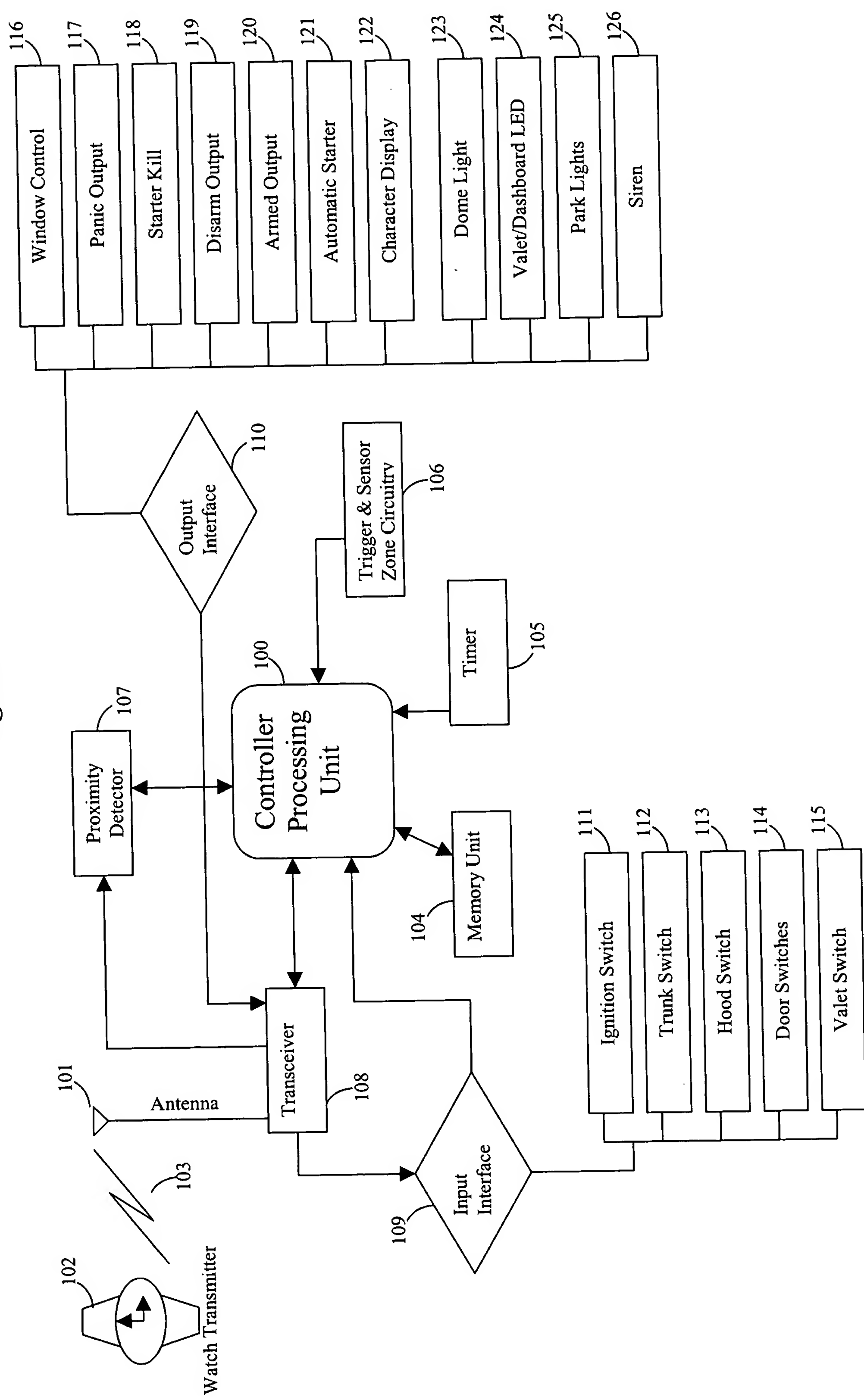


Figure 2

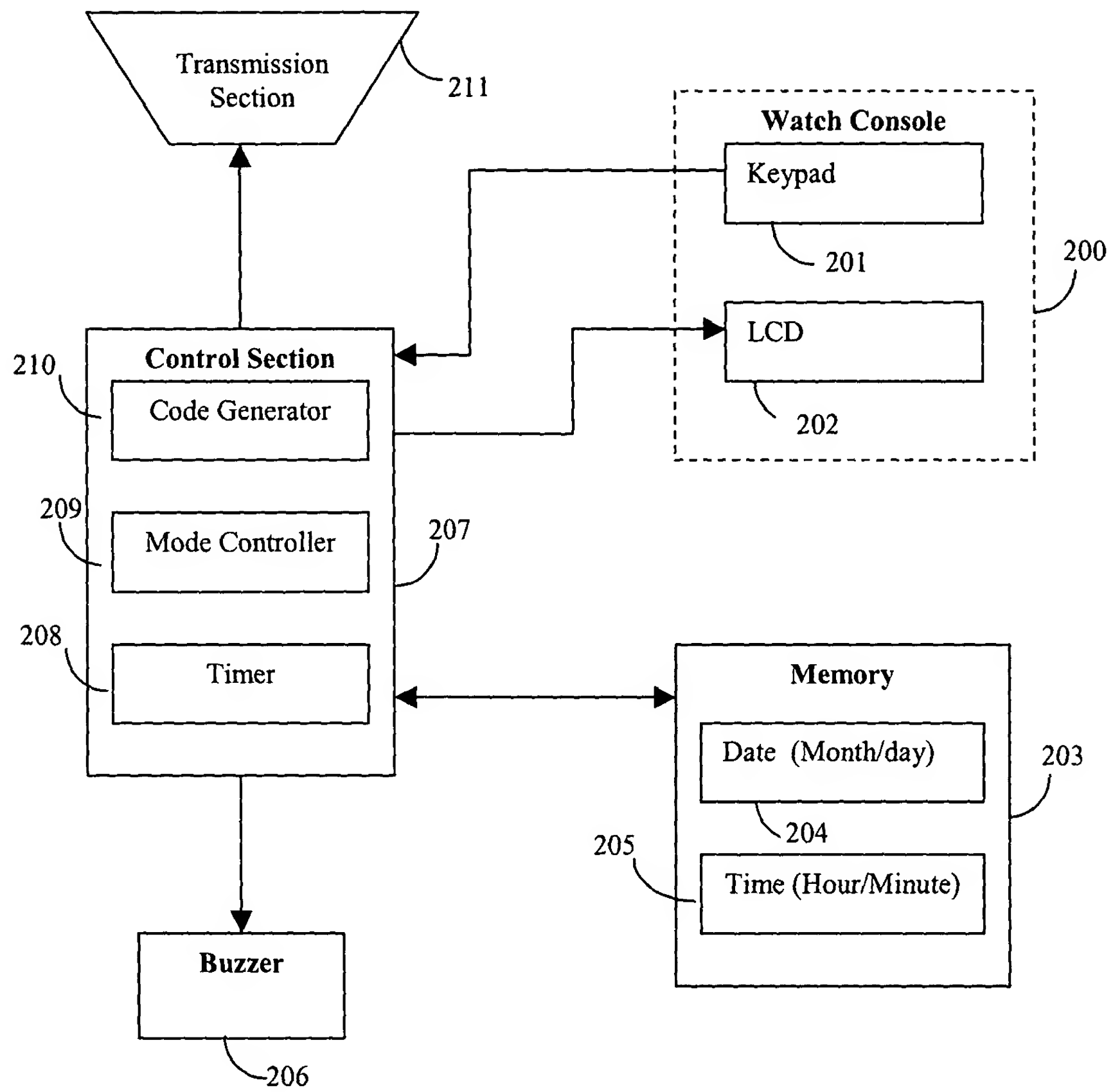


Figure 3

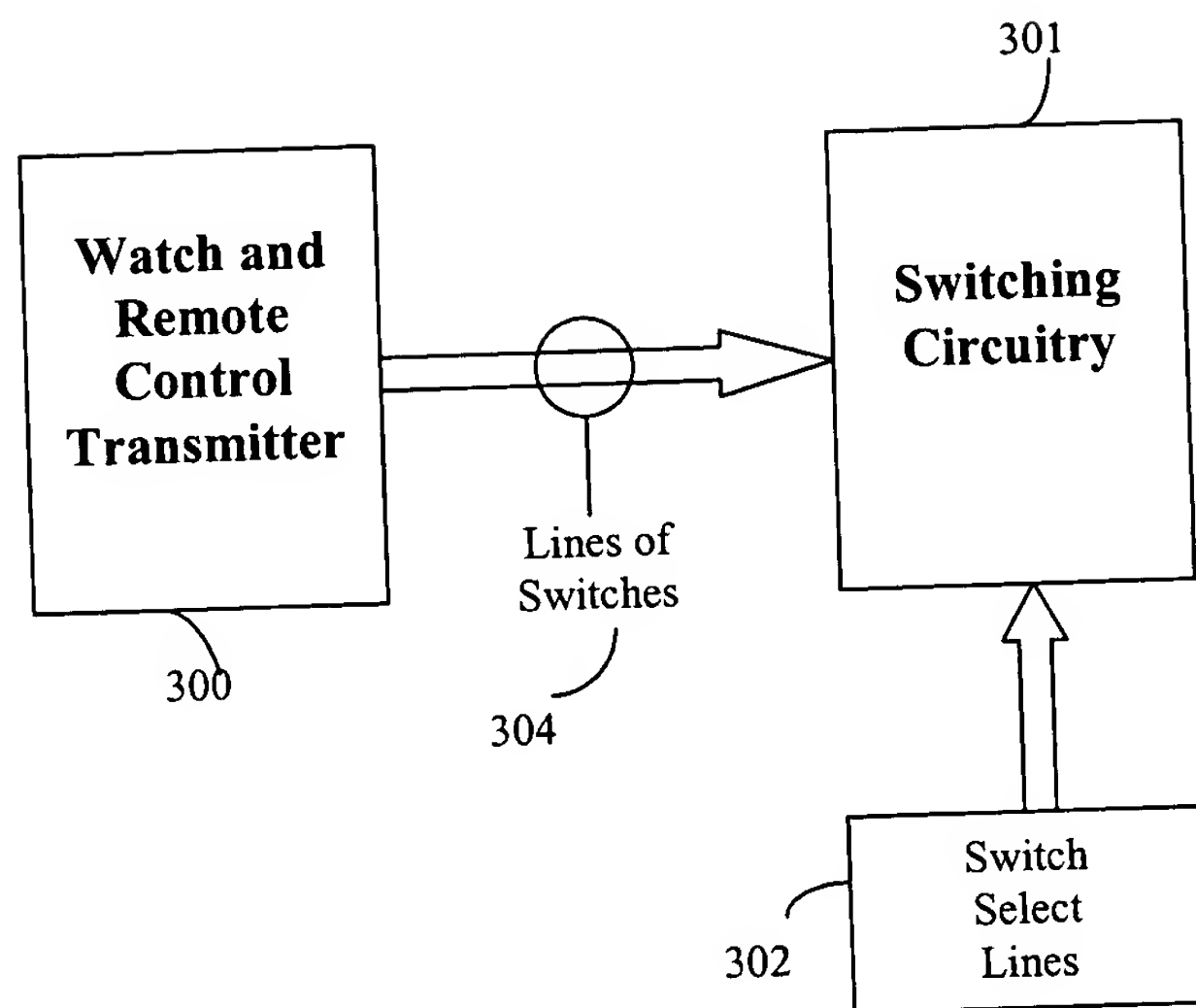
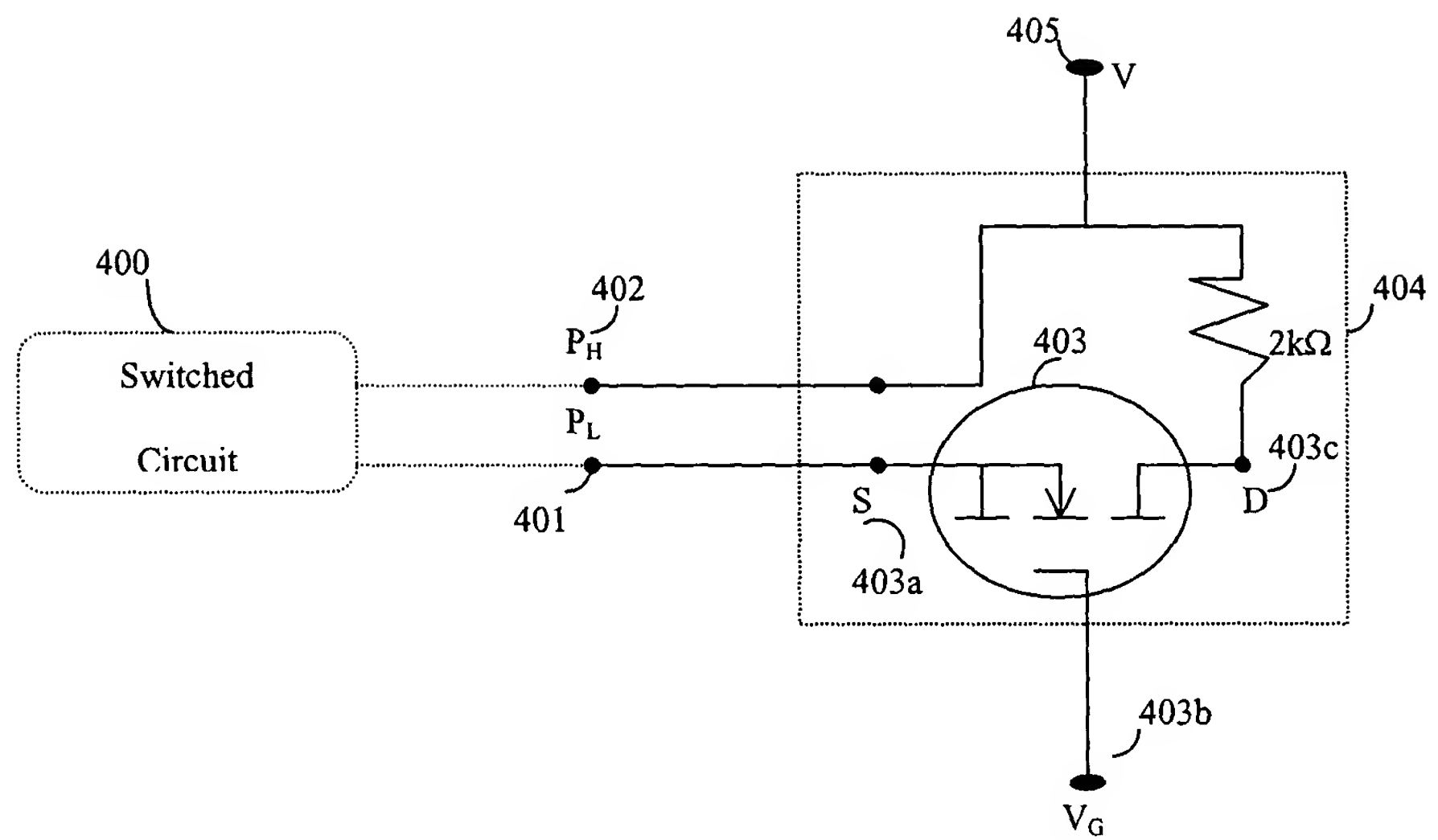


Figure 4

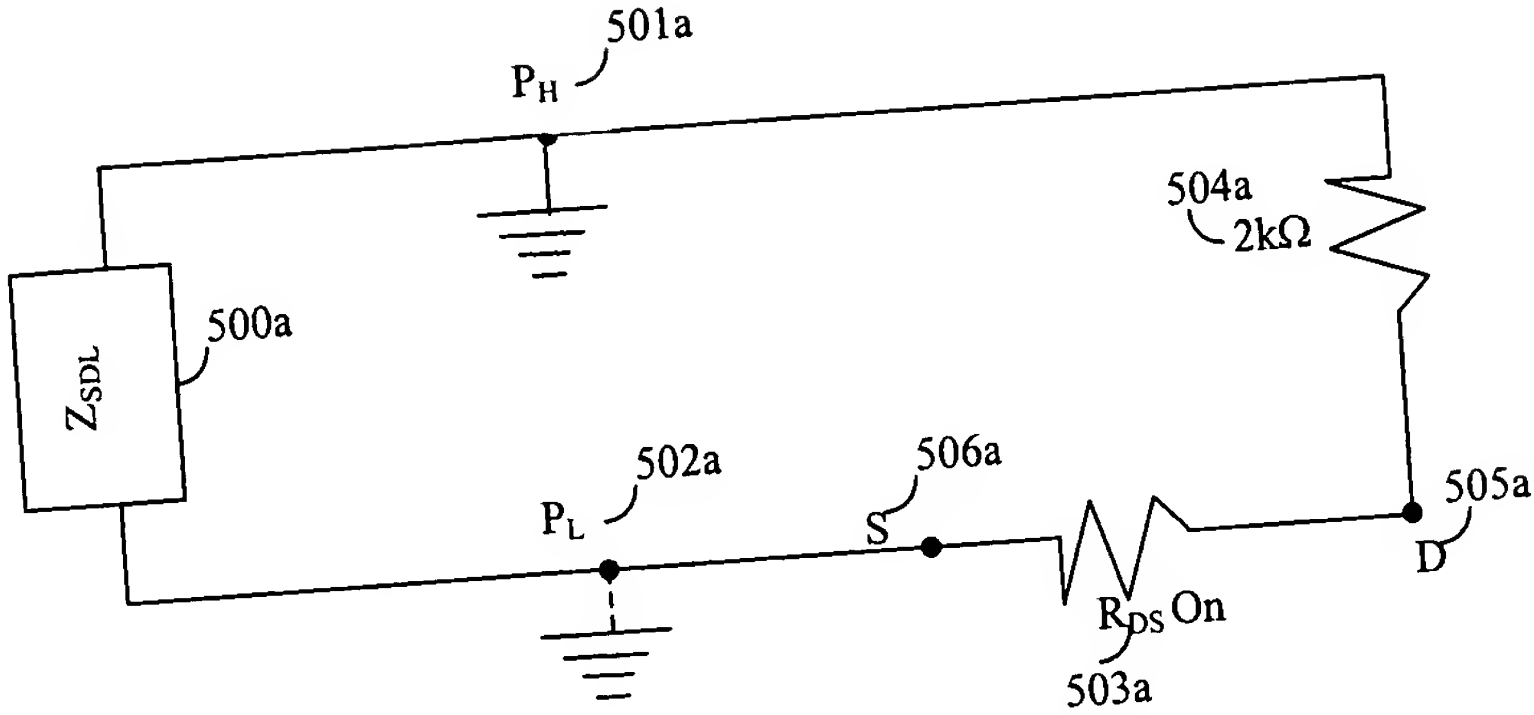


Notes:

- P_L is the low voltage terminal of the switch and the P_H is the high one.
- Q1 is a n-channel enhancement MOSFET

Figure 5

(A) RDS ON



(B) RDS OFF

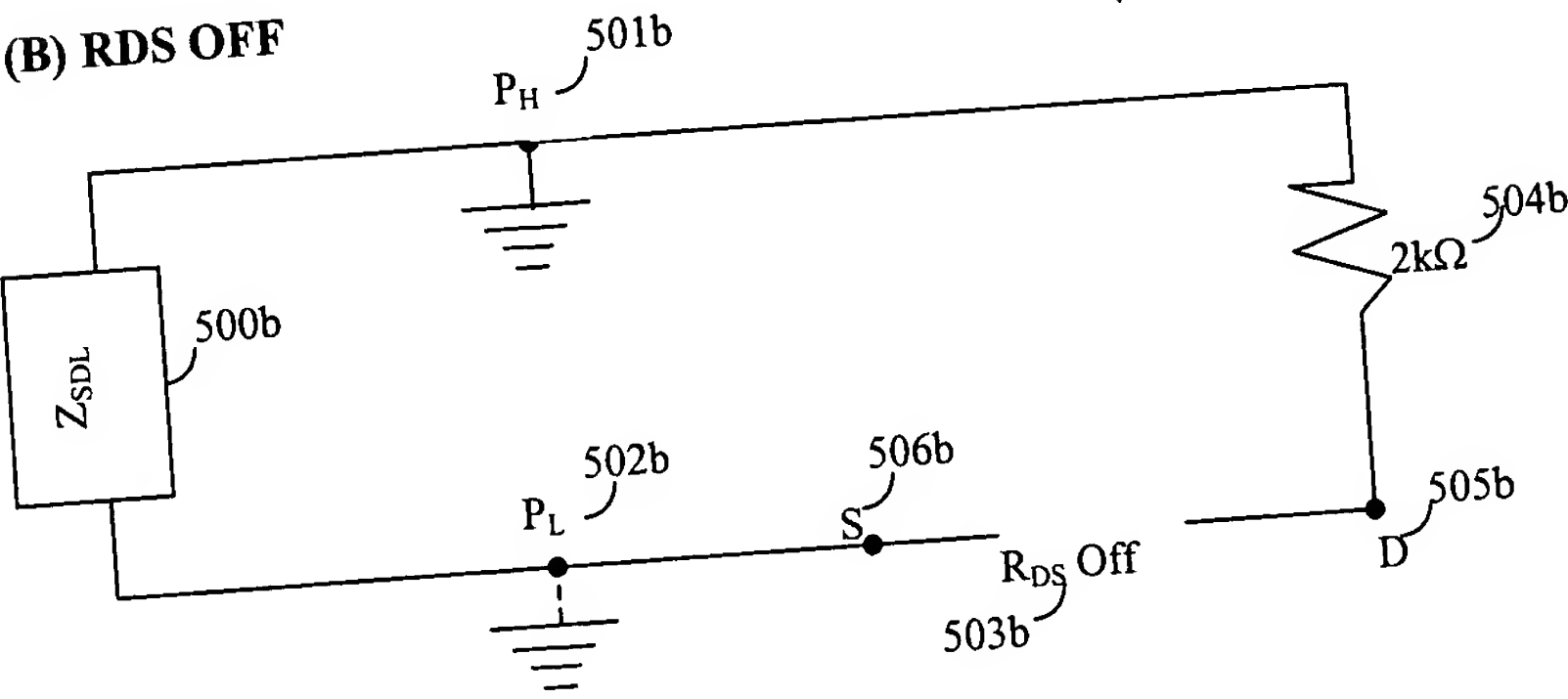
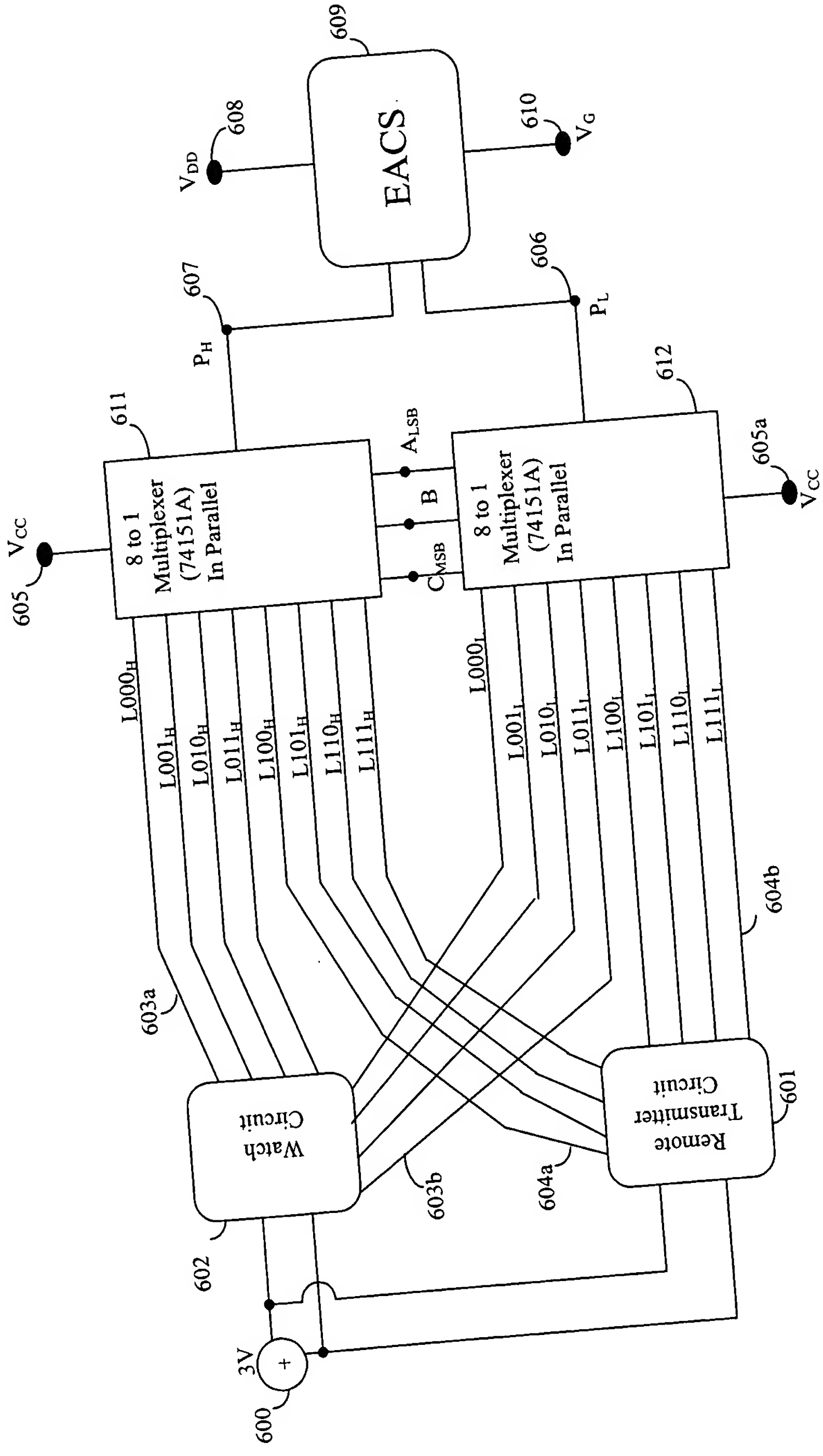


Table 1: Output /Input Levels of EALS

Gate	V _{HL}
0	1
1	0
1 ⇔ 3V	0 ⇔ 3V
0 ⇔ 0V	1 ⇔ non zero
V _{HL} = AC voltage drop from P _H to P _L	
Gate = DC voltage drop to ground	

Figure 6



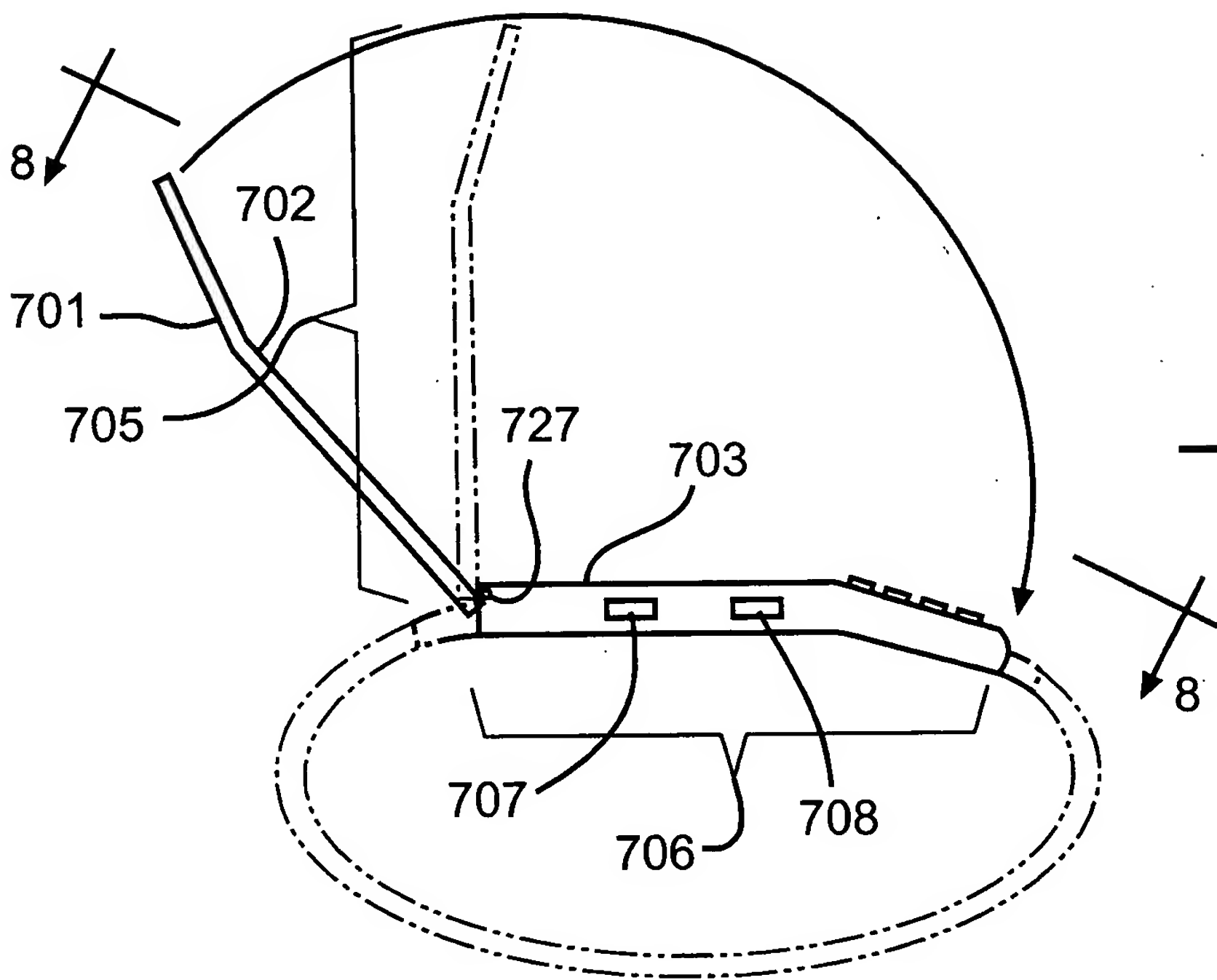


FIG. 7

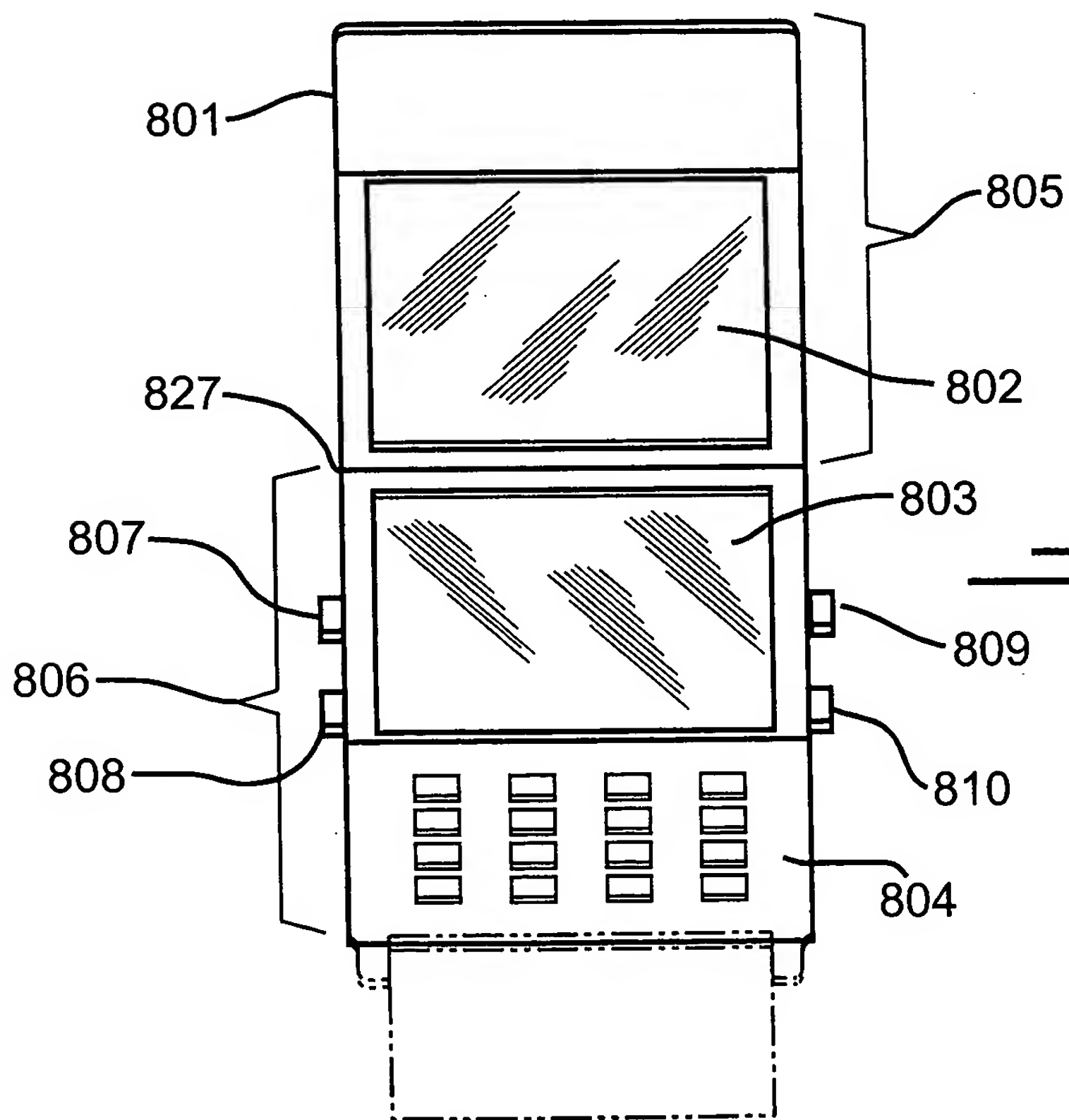


FIG. 8

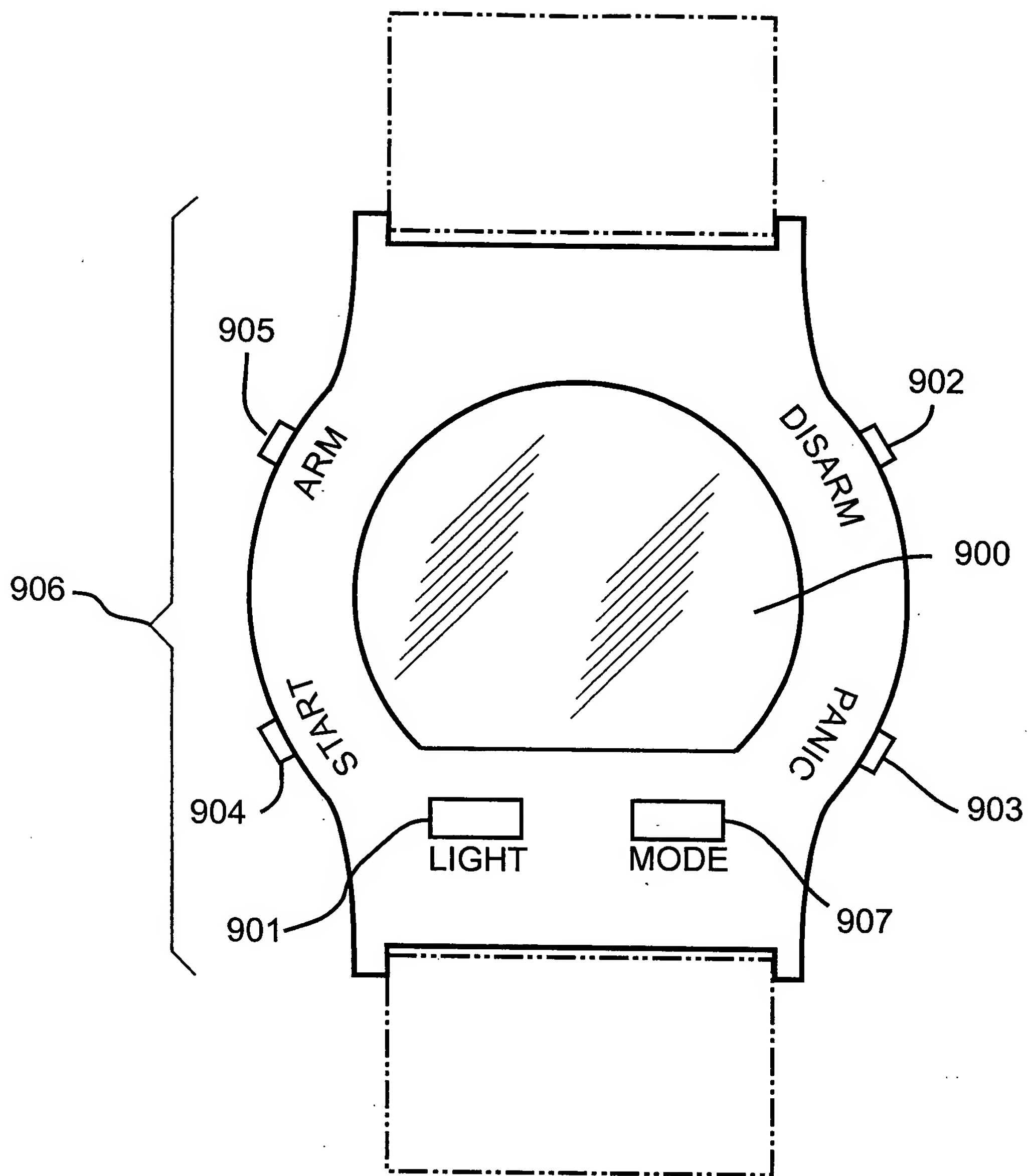


FIG. 9

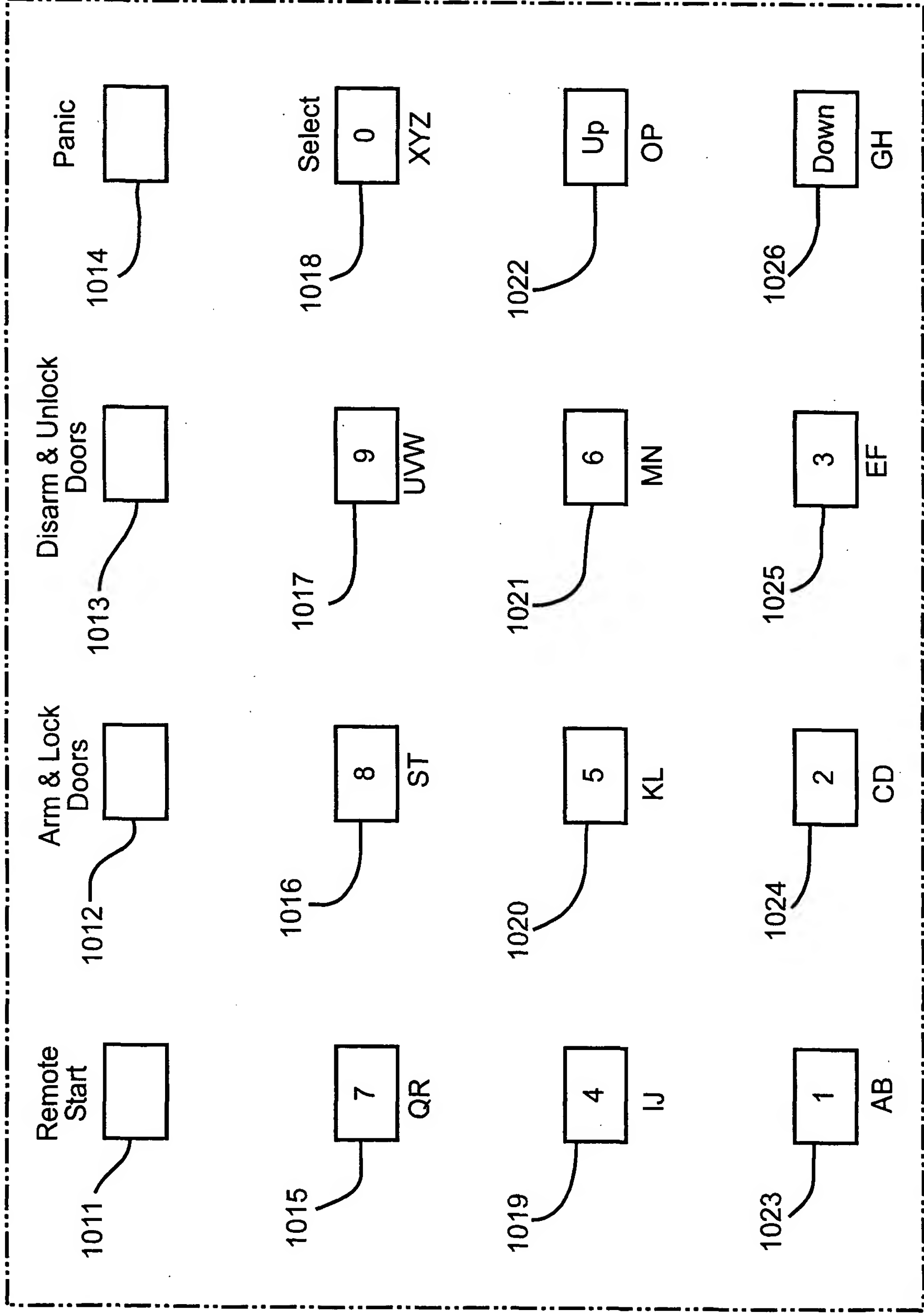


FIG. 10